09/435540

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.:20051128

DATE : November 29, 2005

TO SPE OF : ART UNIT 2152

SUBJECT : Request for Certificate of Correction on Patent No.: 6,970,930

A response is requested with respect to the accompanying request for a certificate of correction.

Please complete this form and return with file, within **7** days to:
Certificates of Correction Branch - PK 3-910
Palm location **7590** - Tel. No. 305-8201

With respect to the change(s) requested, correcting Office and/or Applicant's errors, should the patent read as shown in the certificate of correction? No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Thank You For Your Assistance **Certificates of Correction Branch**

The request for issuing the above-identified correction(s) is hereby:
Note your decision on the appropriate box.

☒ **Approved** **All** changes apply.

☐ **Approved in Part** Specify below which changes **do not** apply.

☐ **Denied** State the reasons for denial below.

Comments:

SPE: Bunjob Jaroenchonwanit **Art Unit** 2152

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 6,970,930 B1
DATED: November 29, 2005
INVENTOR(S): Steven R. Donovan

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Item (56) References Cited,

Please add to the U.S. PATENT DOCUMENTS section the following:

6,324,279 B1	11/2001	Kalmanek, Jr. et al.
6,755,701 B1	8/2004	Pan et al.
6,801,940 B1	10/2004	Moran et al.
6,826,613 B1	11/2004	Wang et al.
6,857,012 B2	2/2005	Sim et al.
2002/0016839 A1	2/2002	Smith et al.
2002/0026513 A1	2/2002	Hoglund et al.

Please add to the OTHER PUBLICATIONS section the following:

Aiken et al., "Network Policy and Services: A Report of a Workshop on Middleware", Internet Engineering Task Force, Request for Comment 2768, February 2000.

Aspnes et al., "On-Line Routing of Virtual Circuits with Applications to Load Balanacing and Machine Scheduling", Journal of the ACM, Vol. 44, No. 3, May 1997, pp. 486-504.

Bhuyan et al., "Impact of Switch Design on the Application Performance of Cache-Coherent Multiprocessors", 1998, http://www.cs.tamu.edu/people/ravi/IPP398.ps.g2.